REMARKS

Entry of this Amendment is proper under 35 U.S.C. §1.116, since no new claims are presented and no new issues are raised. Additionally, Applicants respond to the Examiner's comments in paragraphs 8-10 of the Office Action.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Minor claim amendments are made for grammatical clarity and because the Examiner states in paragraph 10 on page 14 of the Office Action: "... it should be realized that nowhere in claims 14-18 is the limitation of 'a substrate devoid of components'". Although Applicants submit that, to one of ordinary skill in the art, the terminology "wiring interconnect packages" clearly conveys this meaning, claims 14 and 19 have been amended for the benefit of the Examiner's evaluation.

Claims 1-3 and 5-22 are all of the claims pending in the present Application. Claims 1 and 3-7 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,054,863 to Morrison et al, further in view of US Patent 6,288, 561 to Leedy. Claims 14 and 16-18 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,201,383 to Lo et al, further in view of Leedy. Claims 9-13 and 19 stand rejected under 35 USC §103(a) as unpatentable over Lo/Leedy, and further in view of US Patent 5,420,500 to Kerschner.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, e.g., by claim 1, the present invention is directed to an electronic circuit wiring interconnect package test and repair apparatus including at least one wiring analyzer to locate shorts between conductors on a surface of or embedded in a carrier substrate. The carrier substrate includes only conductors at the time of testing. These conductors are intended to interconnect components *that are not yet mounted* on the carrier substrate. A current source provides current sufficient to remove the shorts.

A cluster probe, comprising a plurality of probes, contacts the conductors in a manner controlled by the wiring analyzer.

No cited prior art reference defines a test/repair apparatus for a wiring interconnect package, i.e., a carrier substrate having conductors to interconnect electronic components, wherein the carrier substrate is totally devoid of any such components at the time of testing as defined by the apparatus and process of the present invention.

Advantages of the present invention is that cost and time is considerably reduced for the manufacture of wiring interconnect packages. Indeed, in at least one version of the present invention, a completely automated check of a substrate can be made by making a single contact by the cluster probe to the substrate.

That is, the present invention provides the capability in which a substrate is contacted one time with the cluster probe. The wiring analyzer will check for short and open circuits by systematically taking measurements through predetermined probes of the cluster probe. Without even moving the cluster probe, one or more attempts can then be made to systematically remove any short circuit(s) located by the analyzer, including the optional test of an overvoltage stress test. The substrate is then again re-tested in its entirety, again without moving the cluster probe.

By this novel approach, a substrate can be thoroughly checked out and repaired in a single test apparatus and eliminates even the time-consuming necessity of relocating probes to different locations on the substrate.

II. THE PRIOR ART REJECTIONS

Applicants again submit that the rejection currently of record is unreasonable and improper. The following deficiencies are identified.

1. **The Examiner fails to apply the proper standard of review**. Based on statements in the record, this failure is seemingly because the Examiner continues to fail to recognize the significance of the difference between IC testing/repair versus wiring interconnect package testing/repair.

Applicants have repeatedly stated that, in the art of wiring interconnect package testing, it is not current practice and would be contrary to current industry concepts to combine a test station into a repair station. This current condition in the art is described at line 14 on page 1 through line 16 of page 2 of the specification.

In the rejection, the Examiner reasonably relies on US Patent 6,054,863 to Morrison et al. and US Patent 6,201,383 to Lo et al. as the primary references.

In both of these references, there clearly is no suggestion to combine testing and repair, as clearly described at lines 5-8 of column 5 of Lo: "The results of the testing process are displayed on a display screen 50, and may be used in other ways, such as the diversion of failing components into a scrap bin."

Indeed, the Examiner concedes that neither Morrison nor Lo teaches, suggests, or even hints at, using the testing station for the repair process.

Applicants submit that the reason for the distinction between testing and repair, to one of ordinary skill in the art, is that testing of wiring disconnect packages involves a low voltage (e.g., TTL levels or less) and current (e.g., milliamps) environment, whereas repair requires much higher voltages (e.g., in the present invention, the solid state portion of the apparatus is exemplarily rated at 250 volts, the relay portion is exemplarily rated at up to 1500 volts for stress voltages, and the current range involves tens of amperes).

To one of ordinary skill in the art, a juxtaposition of such diverse range of voltage (e.g., 5 volts versus 1500 volts) and current (e.g., milliamps versus tens of amps) inherently creates a dangerous working environment. It is for this reason that, in this art (e.g., wiring interconnect packaging), it is current practice that the low voltage testing station not be integrated with the high voltage repair station.

This current practice in the art is clearly reflected in both Morrison and Lo.

In an attempt to overcome this deficiency (clearly conceded by the Examiner), Leedy is introduced. However, Leedy involves an entirely different art, testing and repairing integrated circuits.

That is, in contrast to testing/repair of wiring interconnect packaging, the testing and repair of an integrated circuit are both very low voltage and current levels, because low voltage components, including low voltage active components, are already mounted on the

substrate for the testing. Thus, one of ordinary skill in the art would have no concern whatsoever about mixing the testing and repairing environments for an integrated circuit.

It is for this reason alone (e.g., the drastic differences between the two arts in testing versus repair), that Leedy cannot reasonably be combined with either Morrison or Lo.

In the rejection currently of record, words are taken out-of-context from Leedy (e.g., "high voltage or current") in an attempt to maintain the position that these words, which may be "high" in the context of an integrated circuit repair, would suggest to use "high voltage or current" in the environment of repairing wiring interconnect packaging.

However, to one of ordinary skill in the art, the "high voltage or current" in Leedy may not be usable even in the testing station of a wiring interconnect package, let alone in the repair station.

That is, contrary to the Examiner's assertion in paragraph 9 of page 14 of the Office Action, Applicants submit that one of ordinary skill in the art of wiring interconnect packaging would not at all consider that the "high voltage or current" of the IC test set in Leedy would in any meaningful manner satisfy the requirements of the wiring interconnect packing repair stations.

Additionally, in paragraph 8 of page 14 of the Office Action, the Examiner attempts to justify his position that Leedy teaches an extension to "other arts" by pointing to lines 53-63 of column 3 in Leedy: "Other substrates, circuit substrate types, or substrate assemblies that the present invention can process are Multi-Chip Module and flat panel display substrates which may be made from various materials such as AlN, SiC, quartz, glass or diamond".

However, to one of ordinary skill in the art, this description clearly refers to environments that are similar to that of testing/repair of integrated circuits in that low voltage components are already mounted on the substrates in both these scenarios. Therefore, similar to testing/repair of integrated circuits, these environments require similar voltage/current levels for both testing and repairing. Indeed, the term "burn-in" (e.g., see title and abstract of Leedy) is a term of art that requires that components be installed during the testing. The Examiner cannot simply ignore the terms of art in the prior art and present Application.

Thus, in spite of the Examiner's position to the contrary, these words in Leedy would not in any way suggest to one of ordinary skill in the art to combine the low-voltage wiring interconnect package test station that is currently intentionally separated from the inherently dangerous high-voltage repair station.

Stated slightly differently, the rejection currently of record, when properly viewed through the evaluation of one of ordinary skill in the art, fails to reasonably overcome the teaching in the primary references, Morrison and Lo, that clearly reflect the current practice that testing and repair stations are not integrated. One of ordinary skill in the art would also understand that, in this art, this separation is intentionally maintained because of the two drastically different voltage/current conditions.

2. The rejection currently of record fails to provide a proper motivation to combine references.

In paragraph 2 of the Office Action, the Examiner urges a combination of Leedy with Morrison by alleging that it would have been obvious to incorporate Leedy: "... for the purpose (sic) reducing the number of steps and therefore time needed to produce functional boards that are free of defects (column 2, lines 4-9)", "... for the purpose of automatically positioning the cluster probe to reduce the possibility of human error or further damage due to additionally handling", and "... for the purpose of having voltage stress test capability, since it is useful in testing, to make sure a repaired short does not regenerate and to avoid further faults".

In paragraph 3 of the Office Action, the Examiner urges combining Leedy with Lo by additionally alleging that it would have been obvious to incorporate Leedy: "... for the purpose of removing shorts and repairing electronic circuits".

In paragraph 4 of the Office Action, the Examiner urges additionally combining Kerschner with Lo/Leedy by alleging that it would have been obvious to incorporate Kerschner: "... for the purpose of detecting open circuits, since further fault detection is useful in determining the quality of a device under test, and repairing short circuits since it is stated by Lo et al. that 'it is desirable to determine which networks are shorted together, so that the circuit can be repaired'".

All of the above motivations to combine references (plus any others not specifically identified) have the same basic reasoning flaw, as follows: the Examiner merely recites the benefit of the combination if the combination is made.

Stated slightly differently, the rejection of record merely alleges that one would be motivated to combine reference A with reference B because such combination would provide the benefit of having made the combination. That is, the Examiner merely locates words in the secondary reference that describe a feature in that reference. The Examiner then implicitly concludes that the primary reference would likewise benefit from this wording.

The problem with this circular reasoning, in the context of the present invention, is that neither reference suggests applying the element into the environment of the primary reference (e.g., Morrison or Lo).

That is, the Examiner is understood as conceding that Morrison (and, likewise, Lo) makes no suggestion whatsoever to incorporate various features, including repair of the package. Applicants submit that the Examiner has failed to point to any suggestion in any secondary reference (e.g., Leedy or Kerschner) that reasonably suggests to incorporate the feature described in the secondary reference into the entirely different environment of the primary reference (e.g., Morrison or Lo) that fails to have the missing feature.

It is this suggestion that is required for a proper patentability evaluation, not the circular reasoning generated by taking words-out-of-context. The words-out-of-context circular reasoning is nothing but impermissible hindsight. Using the circular reasoning in the rejection currently of record, everything would become obvious by merely locating, in a secondary reference, elements missing from the primary reference and summarily declaring that the combination would be obvious by describing wording in the secondary reference that are not related to the primary reference, absent hindsight.

As stated in the previous Amendment filed July 10, 2003, the rejection of record violates the previously-mentioned evaluation guidelines from MPEP §2143.01.

Stated slightly differently, the rejection of record fails to follow, not only MPEP §2143.01, but also the more basic guideline in §2141.02: "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the

differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious" (emphasis in MPEP itself).

In the present evaluation, Applicants submit that the proper evaluation is whether one of ordinary skill in the art of wiring interconnect packaging would be motivated to contradict the current practice that intentionally separates the low-voltage test station from the high-voltage repair station (and separates them for a very good reason) in the manner done by the present invention.

This is an entirely different evaluation than that of identifying words in isolation and alleging that such words in isolation provide a motivation to modify a reference, since such modification would provide the benefit of these words if the modification were to be done.

Along this line, it is again noted that the purpose of the primary references (e.g., Morrison and Lo) is to test a wiring interconnect package, not to repair the wiring interconnect package. As previously pointed out, one of the guidelines of MPEP §2143.01 prohibits modifications if the principle of operation would change by the modification. It cannot be disputed that repairing a wiring interconnect package is an entirely different principle of operation from that of testing a wiring interconnect package. Other changes in principle of operation were discussed in the previous Amendment filed July 10, 2003, and are not repeated.

3. The combination urged by the Examiner for Morrison cannot reasonably be made for technical reasons.

Finally, Applicants add to the record the following technical explanation as to why Morrison cannot be modified as urged by the Examiner.

It is noted that Thomas Morrison is an inventor in both US Patent 6,054,863 to Morrison et al. and in the present invention. It is noted that the system in Morrison '863 must very accurately measure a small capacitance. This measurement circuit is very sensitive to stray capacitance which would be difficult, if not impossible, to predict or control if additional wiring for the repair feature were to be added. Moreover, in this system, the measurement circuit must be physically very close to the probe, making it difficult to be able to add the switching capability that would be required to add the repair feature.

The Examiner relies on Kerschner to demonstrate a technique for locating open circuits, and so Kerschner does not overcome the deficiencies in Morrison '863 or Lo.

Hence, turning to the clear language of the claims, in either Morrison '863 or Lo, there is no teaching or suggestion of: "... wiring interconnect package test and repair apparatus, comprising: at least one wiring analyzer to locate shorts between conductors, said conductors being on a surface of or embedded in a carrier substrate, said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit, said carrier substrate being devoid of all said components; a current source to provide current sufficient to remove said shorts ... ", as required by claim 1. The remaining independent claims have similar language.

For any of the reasons stated above or in the previous Amendment, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too, even in combination with the Morrison, Lo, Leedy, or Kerschner, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3 and 5-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 12/8/03

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 this Amendment under 37 CFR §1.116 to Examiner T. Dole on December 8, 2003.

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